

# Single-Thread Processor

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40			
PC	A	B	C	D	E	E	E	E	E	E	E	F	F	F	F	F	F	G	G	G	G	H	H	H	H	H	H	H	I	I	I	I	I	I	J	J	J	J	J	J			
FETCH	A	B	C	D	D	D	D	D	D	D	D	E	E	E	E	E	E	F	F	F	F	G	G	G	G	G	G	G	H	H	H	H	H	I	I	I	I	I	I	I			
DECODE			A	B	C	C	C	C	C	C	D	D	D	D	D	D	E	E	E	E	E	E	F	F	F	F	F	F	G	G	G	G	H	H	H	H	H	H	H	H			
OPERAND				A	B	B	B	B	B	B	C	C	C	C	C	C	D	D	D	D	D	D	E	E	E	E	E	E	E	F	F	F	F	F	F	G	G	G	G	G	G		
EXECUTE				A							B						C						D						E														
ADDRESS					A							B						C						D						E							F						
MEM						A						B							C					D							E						F						
MEM							A						B						C						D						E							F					
MEM								A						B						C						D						E								F			
WRITEBACK									A						B							C						D						E							F		
memory in use							1	1	1			1	1	1	1			1	1	1	1				1	1	1	1			1	1	1					1	1	1	1	1	1

Figure 1a

# Single-Thread Processor with Data Cache

machine cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
PC	A	B	C	D	E	E	E	F	F	F	G	G	G	H	H	I	I	I	J	J	J	K	K	K	L	L	L	L	M	M	M	N	N	N	O	O	P	P	P	P
FETCH	A	B	C	D	D	D	E	E	E	E	F	F	F	G	G	H	H	H	I	I	I	J	J	J	K	K	K	L	L	L	M	M	M	N	N	N	O	O	P	P
DECODE			A	B	C	D	D	D	D	D	E	E	E	F	F	F	G	G	G	H	H	I	I	I	J	J	J	K	K	L	L	L	M	M	M	N	N	O	O	
OPERAND			A	B	C	B	B	C	C	C	C	D	D	E	E	E	F	F	F	G	G	G	H	H	I	I	I	J	J	J	K	K	L	L	L	L	L	M	M	M
EXECUTE				A			B	B	C	C	C	D	D	E	E	E	F	F	F	G	G	G	H	H	I	I	I	J	J	J	K	K	L	L	L	L	L	L	L	L
ADDRESS					A			B	B	B	C	C	D	D	E	E	E	F	F	F	G	G	G	H	H	I	I	I	J	J	J	K	K	L	L	L	L	L	L	L
MEM						A																																		
MEM							A																																	
MEM								A																																
WRITEBACK									A																															
memory in use							1	1	1				1	1	1	1			1	1	1				1	1	1	1				1	1	1					1	1

Figure 1b

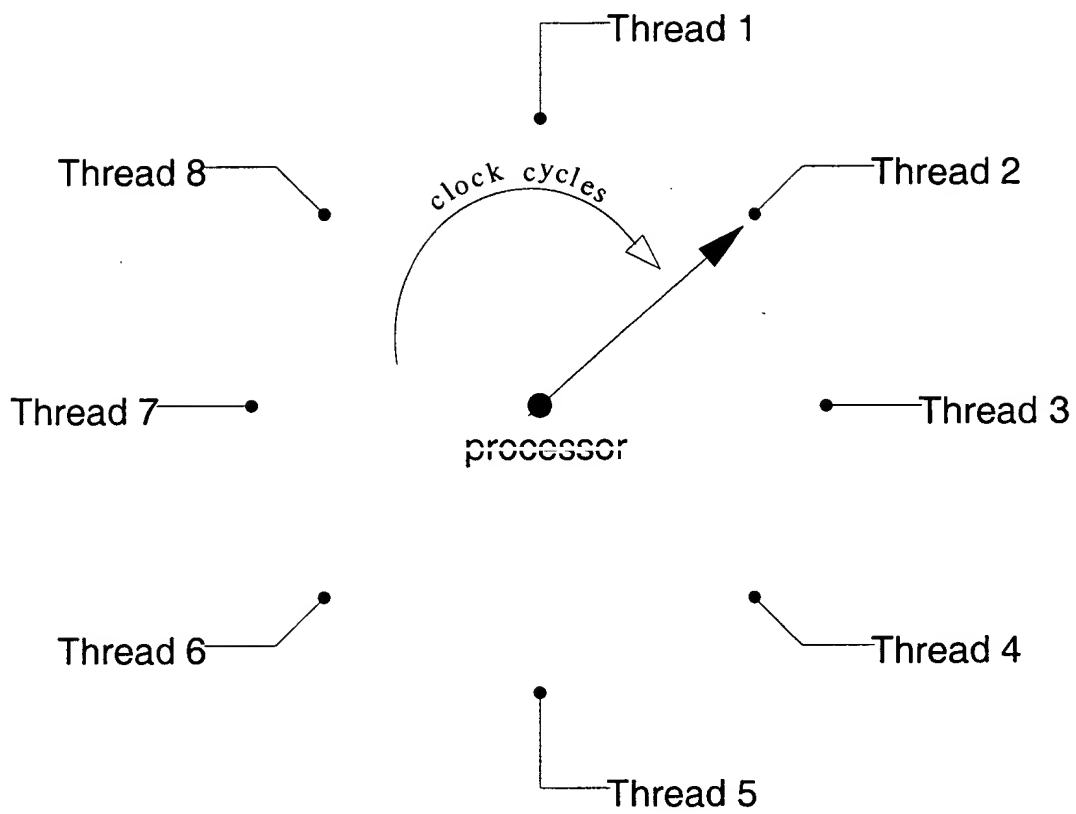


Figure 2

Figure 3a: Four-Thread Processor. This diagram illustrates the internal structure of a four-thread processor, showing the flow of data and instructions between various components. The components are organized into four main sections, each representing a different thread or stage of the processing pipeline. The flow is indicated by arrows, showing the sequence of operations from input to output.

Four-Thread Processor

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
FETCH		1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E
DECODE			1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E
OPERAND				1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E
EXECUTE					1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D
ADDRESS						1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D
MEM							1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D
MEM								1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D
MEM									1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C
WRITEBACK										1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C
memory in use																				

Figure 3a

Four-Thread Processor with Banked Memory

active thread	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
PC	1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E	4E
FETCH		1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E	3E
DECODE			1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E	2E
OPERAND				1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D	1E
EXECUTE					1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D	4D
ADDRESS						1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D	3D
MEM							1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D	2D
MEM								1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C	1D
MEM									1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C	4C
WRITEBACK										1A	2A	3A	4A	1B	2B	3B	4B	1C	2C	3C
memory1 in use																				
memory2 in use																				

Figure 3b

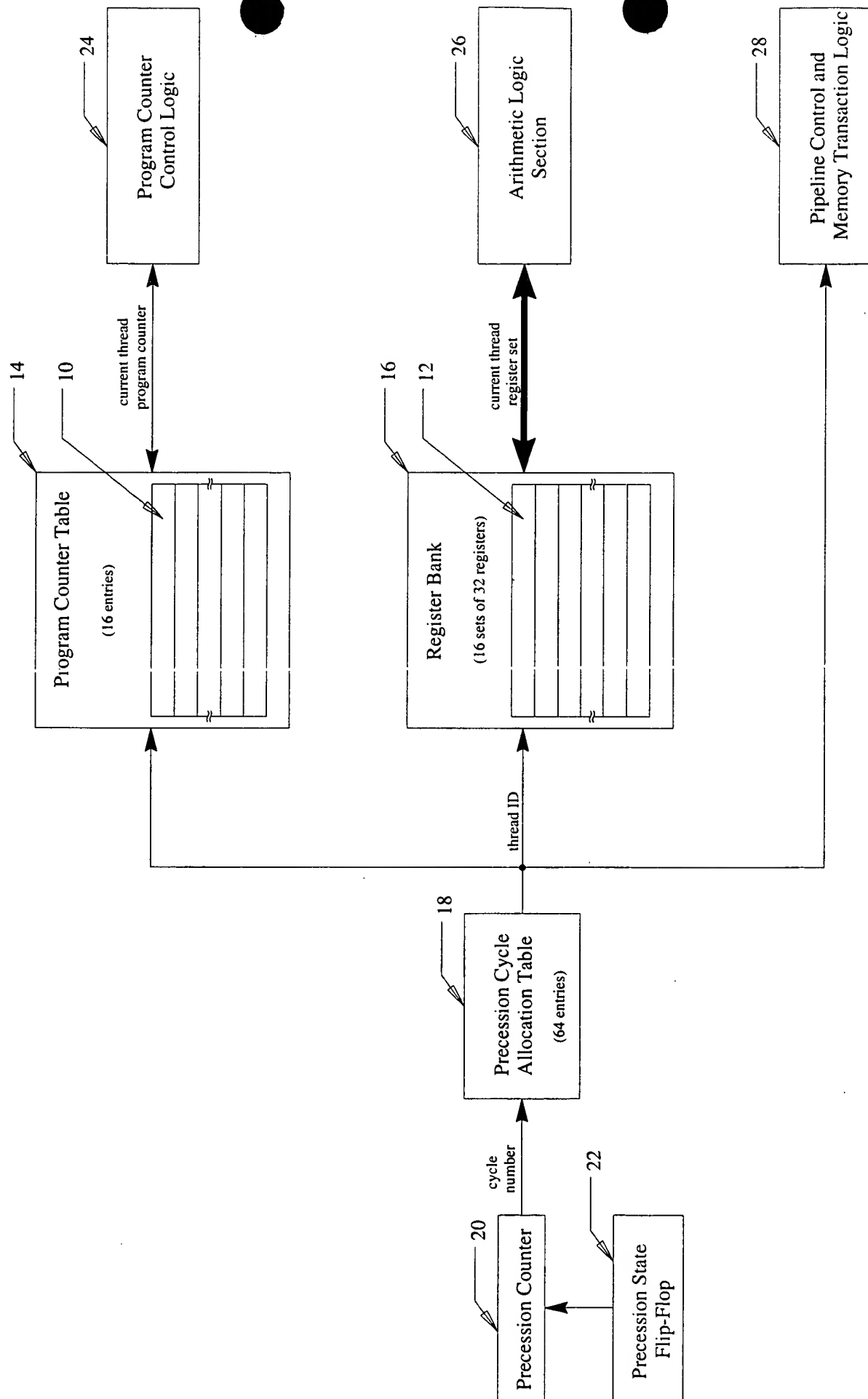


Figure 4

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

commutator

Cycle Allocation Table

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 . . .

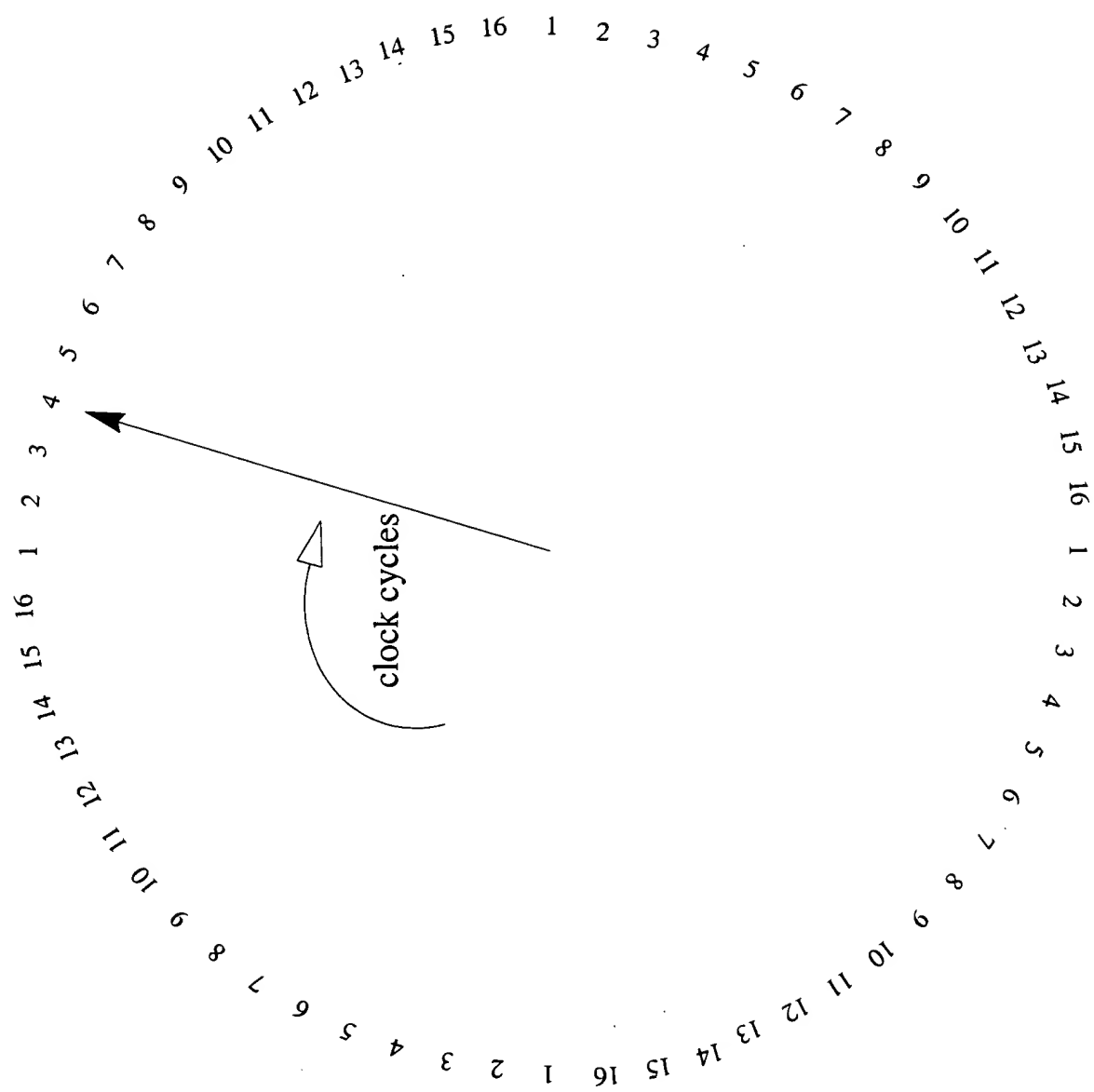


Figure 5

Figure 6

# Cycle Allocation Table

commutator

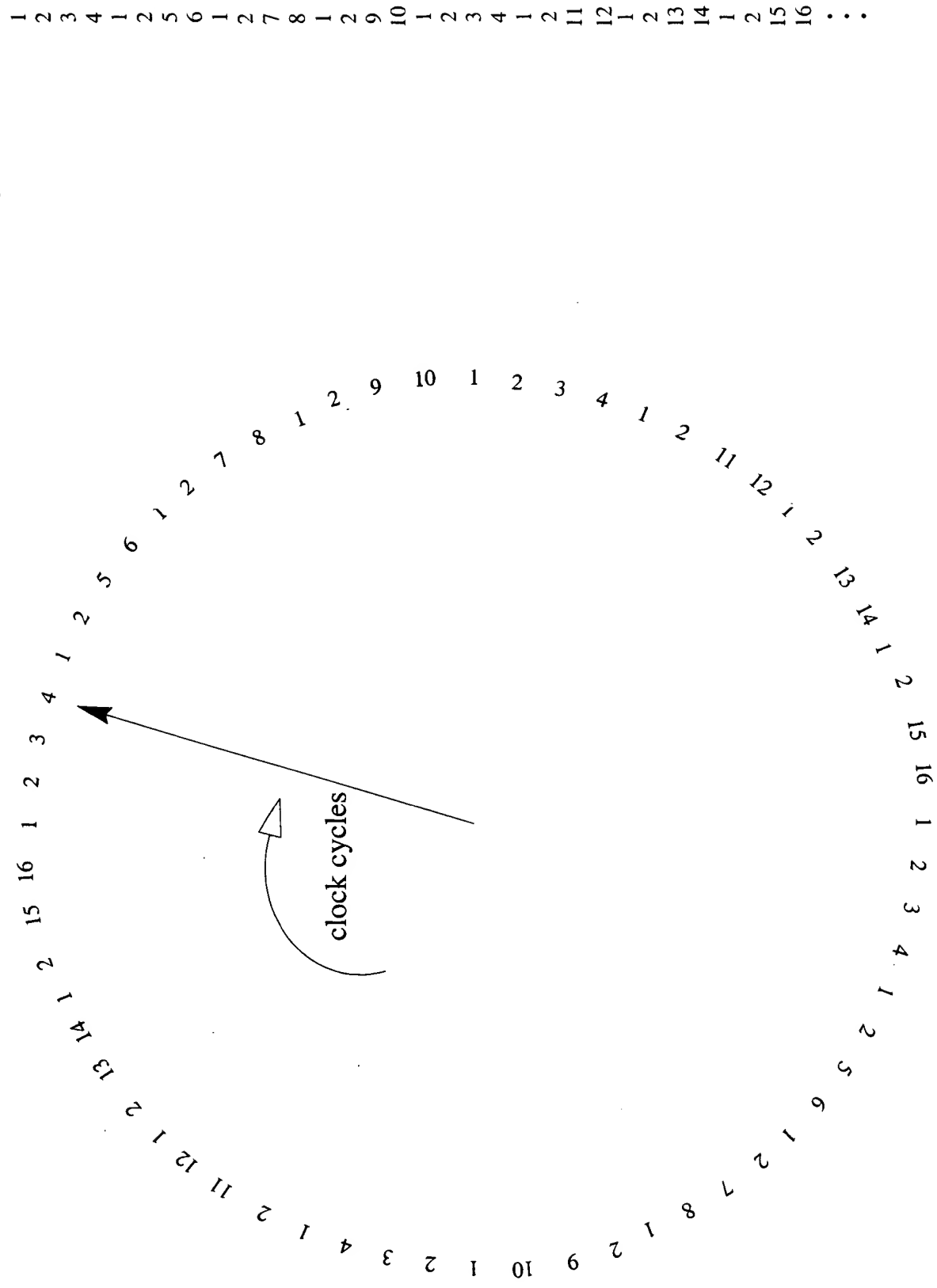


Figure 6